ABSTRACT OF THE DISCLOSURE

Presented is a memory cell integrated in a semiconductor substrate that includes a MOS device connected in series to a capacitive element. The MOS device has first and second conduction terminals, and the capacitive element has a lower electrode covered with a layer of a dielectric material and capacitively coupled to an upper electrode. The MOS device is overlaid by at least one metallization layer that is covered with at least one top insulating layer. The capacitive element is formed on the top insulating layer. The cell is unique in that the metallization layer extends only between the MOS device and the capacitive element.

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